



Air Force Research Laboratory Space Vehicles Directorate Spacecraft Performance Analytics and Computing Environment Research (SPACER)

Description of Technology:

Space processor technologies typically lag their commercial counterparts by several technology node generations. Moreover, the commercial computing landscape has become increasingly complex owing to the rapid evolution of many specialized high performance architectures such as Field Programmable Gate Arrays, Graphics Processing Units, Digital Signal Process and heterogeneous hardware architectures that offer significant advantages over conventional microprocessors.

To leverage these capabilities for space, the Air Force Research Laboratory's (AFRL) Space Vehicles Directorate (RV) has established an in-house computing architecture laboratory known as the Spacecraft Performance Analytics and Computing Environment Research (SPACER) testbed to characterize the utility of these diverse architectures for space applications.

The SPACER testbed is equipped with commercial state-of-the-art and space grade processing platforms, which enables AFRL researchers to characterize the performance of sensitive application codes and lower level computational algorithms on relevant hardware. The development boards are networked together, when possible, to enable distributed computing applications across multiple platforms. The testbed has development workstations, hosting the development tools needed for programming the boards, in an enclave within the Defense Research and Engineering Network (DREN) to allow collaboration within AFRL.

Space
Vehicles
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Stay One Step
Ahead In
Space



Some of the development platforms available in the SPACER laboratory



2016 AFRL Space Scholars in the SPACER laboratory

Exploring methods to address demands for greater levels of on-board computation in next generation defense and scientific satellite missions

In addition to processor architecture research, SPACER activities include spacecraft architecture modeling and simulation. The SPACER team has built a software tool that enables researchers to create a detailed hierarchical description of a satellite architecture — down to the individual component level, if desired — and analyze its performance in various mission scenarios.

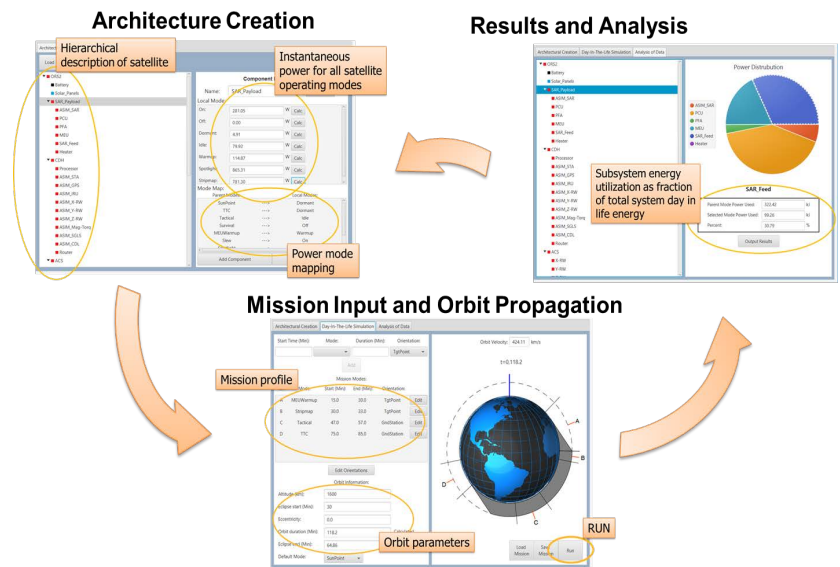
The software enables researchers to describe a mission profile (i.e., a set of orbit parameters and a sequence of orbital operating modes/activities). From this information, the model performs a discrete event simulation to compute the energy expended during the orbit. The model provides the capability to quickly and easily modify the inputs and spacecraft configuration and re-run the simulation — enabling one to generate a trade-space that captures satellite energy expenditures as a function of architecture description and mission profile.

Need for Technology:

As AFRL looks ahead to the requirements of next generation of scientific and defense satellites, there is a clear indication that the need for on-board processing will be dramatically greater than the processing performed presently. This is due to the desire for greater levels of on board autonomy coupled with the development of more advanced sensor technologies that produce far more raw data than can be transmitted to the ground, necessitating greater levels of on-orbit image processing and data compression.

Collaboration:

The SPACER research team is engaged in collaborations with the Space and Missile Systems Center to study processing options for ISR algorithms, the National Science Foundation's Center for High Performance Reconfigurable Computing for the development of device metrics and kernel benchmarks, and the University of New Mexico for mapping of application codes to computing hardware platforms. The team also supports cross-division collaborations within RV including support to the Battlespace Environment Division for optimization of their HTI algorithm, and support to the Integrated Experiments and Evaluation Division for modeling and simulation of CubeSat architectures.



Spacecraft architecture modeling tool being developed in the SPACER laboratory

The SPACER architecture testbed will aid in the identification of computing technologies that can be adapted for use in space to enable desired level of on-board processing for next generation mission needs. This will allow us to bridge the performance gap between these mission application needs and currently available space computing resources.

The spacecraft modeling and simulation capability we are developing addresses a longstanding need to quantify the impact of component-level hardware decisions at the satellite system level. This capability will enable creation of a detailed trade-space comparing the benefits resulting from improvements in dissimilar components — providing stronger justification for investment decisions in new technologies.